Last DSM Algorithm
AUX Version

02/12/ 2004

Input Bits

Input Channel	Bit Description
0	CTB Multiplicity Bits 0:15–Multiplicity
1	VTX Information Bit 0–BBC TAC difference in window Bit 1–ZDC TAC difference in window Bit 2–BBC East small-tile ADC sum over threshold 0 Bit 3–BBC West small-tile ADC sum over threshold 0 Bit 4 -- BBC East large-tile ADC sum over threshold 0 Bit 5 -- BBC West large-tile ADC sum over threshold 0 Bit 6–ZDC East ADC sum over threshold 0 Bit 7–ZDC West ADC sum over threshold 0 Bit 8–ZDC East TAC in window Bit 9–ZDC West TAC in window Bit 10–ZDC East+West attenuated sum over threshold Bits 11:13–Unused Bit 14 - ZDC East ADC sum over threshold 1 Bit 15 - ZDC West ADC sum over threshold 1
2	CTB upper output bits Bit 14: UPC topology
3	EMC Information Bits 0:1 - Unused Bits 2:3–BEMC high-tower bits Bit5–J/Ψ bit from BEMC-high towers Bits 4:8 - Unused Bits 9:10–EEMC high-tower bits Bits 11:15 - Unused
4	Miscellaneous Information Bit 0–Blue bunch filled Bit 1–Yellow bunch filled Bits 2:15 - Unused
5	FPD Information Bit 0–FPD trigger conditions met Bits 1:15 - Unused
6	Special Trigger Requests Bits 0:2–selected special trigger request (zero if no request) Bits 3:6–detector number (0:15) of detector making request Bits 7:13–Unused Bit 14–Zero-bias bit Bit 15–Random bit
7	Unused

Registers

Register	Register Description

0	16-bit low threshold for the CTB Multiplicity
1	16-bit medium threshold for the CTB Multiplicity
2	16-bit high threshold for the CTB Multiplicity
3	16-bit low threshold for the CTB Multiplicity Window
4	16-bit high threshold for the CTB Multiplicity Window

Output Bits

Bit	Description
Bits 0:14	If Bit 15 = 1–Special Trigger Requests Bits 0:2–Special Trigger request Bits 3:6–Special Trigger detector Bit 7–Random bit Bits 8:15–Unused, set to 1 Else–Physics Data Bits 0:1–two bits encoding a number between 0 and 3 indicating which of three multiplicity thresholds was passed Bit 2–BBC TAC difference in window Bit 3–ZDC TAC difference in window Bit 4–Both BBC small-tile ADC sums over threshold Bit 5–Both ZDC ADC sums over threshold Bit 6–Both ZDC TACs in window Bit 7–ZDC East+West attenuated sum over threshold Bit 8 - Zero-bias bit Bit 9 - Blue bunch filled AND yellow bunch filled Bit 10–Any BBC large-tile ADC sum over threshold Bit 11–BEMC high-tower bit2 (second threshold) Bit 12–UPC: (th0 < ZDC E/W ADC <= th1) and (CTB window or topology) Bit 13–EEMC high-tower bit2 (second threshold) Bit 14–BEMC J/Ψ
Bit 15	Flag indicating meaning of bits 0:14
Bits 16:31	Same definitions as bits 0:15

Internal Logic

- The CTB multiplicity is compared to five thresholds whose values are set during RUN configuration (Regs. 0, 1, 2, 3 and 4). The CTB multiplicity is inside the UPC window if it is greater than the threshold set in register 3 and less than the threshold set in register 4.
- A decision is made to pass Physics Data or a Special Trigger Request to the TCU.
    1. The 3 bits of the special trigger request and the random bit are OR'ed together
    2. If ANY of these bits is"1"then output bit 15 will be 1, and the special trigger request and the random bit will be passed to the TCU.
    3. If NONE of these bits is"1"then output bit 15 will be 0 and any physics data will be passed to the TCU.